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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,163	01/26/2004	Min-Su Kim	2557-000188/US	6721
30593	7590	09/15/2005	EXAMINER	
HARNES, DICKEY & PIERCE, P.L.C.			NGUYEN, VIET Q	
P.O. BOX 8910			ART UNIT	
RESTON, VA 20195			PAPER NUMBER	
			2827	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/763,163

Applicant(s)

KIM, MIN-SU

Examiner

Viet Q. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Election filed on 8/15/2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-22 is/are allowed.
- 6) ☒ Claim(s) 23-26 is/are rejected.
- 7) ☒ Claim(s) 27 and 28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/10/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. In response to applicant's remarks, the last restriction requirement is now withdrawn, and all claims **1-28** are present for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **23 and 26** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Magome (US 5,566,128)**, or **Taguchi (US 6,339, 273)**, or **Proebsting (US 6,104,653)**.

Magome (see Fig. 5A) teaches a memory circuit including sensing and decoder apparatus, and Fig. 5C further shows the use of at least two column select signals SCSL0 & SCSL1 (as the applicant's claimed selection signals) for selecting and coupling the corresponding at least two signal pairs (data lines DQ0 & DQ2) to the sense amplifier circuit (S/A). Thus, the sense amplifying circuit will amplify only the signal pairs that is selected and turned on by one of these column select lines (SCSL)> It should be noted that although there are only show two select lines in Fig. 7, Fig. 5

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shows that are more than two said pair select signals and these signals are controlled by the decoder and column addressing circuitry as well-known to one skilled in this art, see also Fig. 6.

Similarly, **Taguchi (see Fig. 1)** teaches a memory circuit including a sensing apparatus (SA) for selecting only one signal pair either the left signal pair (BL1, BL1X) coming from the left-side memory array) or the right signal pair (BL2, BL2X) coming from the right-side memory array) under control of the selection or switch signals (SW1 to SW4). Note that col. 4 (lines 65-67) state that both switches (SW1, SW2) are activated at same time, or alternatively both switches (SW3, SW4) are activated at same time. Furthermore, 3 clearly shows the detailed switching arrangement using clock/control/selection signals (BT1 or BT2) for either memory arrays (CAR1 or CAR2), respectively for selecting and coupling the corresponding at least two signal pairs (left and or right data lines pair BL, BLX) to the sense amplifier circuit (S/A in the middle). Thus, the sense amplifying circuit will amplify only the signal pairs that is selected and turned on by one of these clock select lines (BT1 or BT2);

Similarly, **Proebsting (see Fig. 2)** teaches a memory circuit including a sensing apparatus (SA) for selecting only one signal pair either the top signal pair (BL, BLB) coming from the top-side memory array) or the bottom signal pair (BL, BLB) coming from the bottom-side memory array) under control of the selection or switch signals (ASU or ASD). Thus, the sense amplifying circuit will amplify only the signal pairs that is selected and turned on by one of these column select lines (ASD or ASU);

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4. Claims **23-26** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Volelsang et al (US 6,049,492)**.

Regarding claims **22 & 26**, **Volelsang (see Fig. 1)** teaches a memory circuit including a sensing apparatus (Sat, Sac), and Fig. 1 further shows the use of at least two MUX select signals MUXa & Muxb (as the applicant's claimed selection signals) for selecting and coupling the corresponding at least two signal/bit pairs (either the left data line pair BLta, BLca, or the right data pair lines BLtb, BLcb) to the sense amplifier circuit (S/A) in the middle. Thus, the sense amplifying circuit in the middle will amplify only the signal pairs that is selected and turned on by one of these control/select lines (MUXa or MUXb).

Regarding claims **24-25**, Fig. 3 timing diagram shows that while one of the MUX select signal (i.e., MUXa) has a high potential/logic level to enable the left array, the other MUX select signal (i.e., MUXb) has a low potential/logic or inverted/opposite to the previous one to isolate the right array. Thus, these MUX select signals are shown as inverted corresponding to each other and thus they can be obtained or produced by the associated MUX selection circuitry and/or clocks as also well-know and inherent to one skilled in this art.

5. Other claims contain allowable subject matter over the prior arts of record for the reasons as stated below:

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- Claims **1-22** all recite a particular sensing amplify circuitry which includes the particular connection structure, and the particular use of latching and switching units, which are either not shown or fairly suggested elsewhere;
- Claims **27-28** are objected as being dependent upon reject base claims (**23 & 26**), however, they recite the particular steps of sensing method using precharging and controlling the voltage levels of the sensing nodes in a way that prior arts lack.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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V. Nguyen
09/12/2005



VIET Q. NGUYEN
PRIMARY EXAMINER